Docket No.: MUH-12624

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By: _____ Date: ___December 12, 2003___

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicant	: Martin Freitag, et al.
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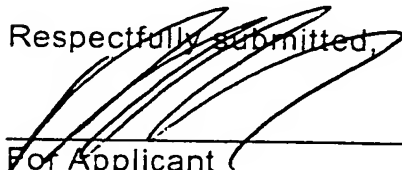|	
Docket No.	: MUH-12624
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CLAIM FOR PRIORITY

Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450

S i r :

Claim is hereby made for a right of priority under Title 35, U.S. Code, Section 119, based upon the German Patent Application 101 03 313.3, filed January 25, 2001.

A certified copy of the above-mentioned foreign patent application is being submitted herewith.

Respectfully submitted,

_____
For Applicant

Date: December 12, 2003

RALPH E. LOCHER
REG. NO. 41,947

Lerner and Greenberg, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101

/av

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Prioritätsbescheinigung über die Einreichung
einer Patentanmeldung

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Anmelder/Inhaber:	Infineon Technologies AG, München/DE
Bezeichnung:	MRAM-Anordnung
IPC:	H 01 L, G 11 C

Die angehefteten Stücke sind eine richtige und genaue Wiedergabe der ursprüng-
lichen Unterlagen dieser Patentanmeldung.

München, den 26. September 2003
Deutsches Patent- und Markenamt
Der Präsident
Im Auftrag

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Applic pgs ... Rule 53b New ☐ Contin ☐ Div ☐ CIP ☐ / Rule 53c Prov. ☐ / Rule 53d CPA ...RCE ☐
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Docket No.: MUH-12624

C E R T I F I C A T I O N

I, the below named translator, hereby declare that: my name and post office address are as stated below; that I am knowledgeable in the English and German languages, and that I believe that the attached text is a true and complete translation of

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Hollywood, Florida

Christine Kahl

April 21, 2004

Lerner & Greenberg, P.A.
P.O. 2480
Hollywood, FL 33022-2480
Tel.: (954) 925-1100
Fax.: (954) 925-1101

Description

MRAM Arrangement

The present invention relates to an MRAM arrangement (MRAM = magnetoresistive RAM) comprising a multiplicity of memory cells which are arranged in a memory matrix and each of which comprises at least one MTJ layer sequence (MTJ = Magnetic Tunnel Junction) and a selection transistor, of which the MTJ layer sequences are in each case located between word lines and bit lines, which run at a distance from one another, the selection transistors are connected to first select lines at their gates for reading from the memory cells and the MTJ layer sequences are connected to second select lines.

In their simplest embodiment, MRAM arrangements — also called MRAMs for short hereinafter — comprise memory cells which are arranged in a memory matrix and each of which has only MTJ layer sequence in each case. Such an MTJ layer sequence is shown in Fig. 5: a tunnel barrier layer 1 lies between a soft-magnetic layer 2 and a hard magnetic layer 3 and comprises an oxide barrier. The tunnel barrier layer 1, the soft-magnetic layer 2 and the hard-magnetic layer 3 thus form an MTJ layer sequence 4, the electrical resistance of which depends on the orientation of the magnetic moments in the two magnetic layers and 2 and 3. This is because if the magnetizations in the two layers 2 and 3 are oriented parallel to one another, then the resistance of the MTJ layer sequence 4 is low, whereas an antiparallel orientation of said magnetizations produces a higher resistance of the MTJ layer sequence. The determination of the cell content of a memory cell formed from such an MTJ layer sequence is measured by sending a current I through the

MTJ layer sequence 4. The magnitude of this current I can then be used to deduce whether the MTJ layer sequence 4 is in the state of a high resistance (antiparallel orientation of the magnetizations) or in the state of a low resistance (parallel orientation of the magnetizations). Each of these states can then be assigned an information content "0" or "1".

This is illustrated diagrammatically in Fig. 6, in which the magnetic field generated by corresponding currents in the bit lines and word lines is plotted on the abscissa and the normalized resistance value is plotted on the ordinate. It can clearly be seen that the resistance of the MTJ layer sequence 4 is about 15% lower in the case of parallel orientation of the magnetizations than in the case of antiparallel orientation. The parallel orientation of the magnetization is assigned the information content "0" here, while the antiparallel orientation of the magnetization has the information content "1". However, other assignments are also possible, of course.

Memory cells comprising MTJ layer sequences 4 are written to by the orientation of the magnetic moments being set in controlled fashion. For this purpose, the memory cell is positioned between two electrical conductors, namely a bit line BL and a word line WL, as is illustrated in Fig. 7. By then sending suitable currents through these lines BL and WL, it is possible to generate a magnetic field at the location of the MTJ layer sequence 4, that is to say in the memory cell comprising the latter, which magnetic field makes it possible to set the direction of the magnetic moments, that is to say, in particular, the direction of the magnetic moments in the soft-magnetic layer 2. In order to ensure this possibility of setting the magnetic moments in the soft-magnetic layer 2 of the MTJ layer sequence 4, it is generally sufficient if, in

one of the lines BL and WL, the direction of the current flowing through this line can be reversed. Through corresponding changeover of the direction of this current, it is thus possible to switch between parallel and antiparallel orientation of the magnetizations and thus between a low-resistance and a high-resistance state of the memory cell.

The already mentioned simplest conceivable construction of an MRAM arrangement is illustrated in Fig. 8: MTJ layer sequences 4 each forming memory cells lie at the crossover points of word lines WL1, WL2, WL3 and bit lines BL1, BL2, which run parallel in each case. A specific memory cell is written to by sending corresponding currents through the bit line BL2 and the word line WL3, for example. A corresponding magnetic field then prevails at the crossover point between the bit line BL2 and the word line WL3 (that is to say on the far right in Fig. 8) on account of these currents, with the result that the MTJ layer sequence lying there or the memory cell formed by the latter is correspondingly written to.

What is advantageous about the arrangement shown in Fig. 8 is its high-density configuration: in a completely ideal manner, only an area of 4 F^2 is required per information content or bit, where F denotes the minimum feature size of the technology used. However, what may be regarded as a major dis-advantage of such a configuration of an MRAM arrangement is that considerable parasitic currents flow through adjacent cells during read-out on account of the only slight differences in the resistance value (about 15%; cf. above), with the result that such an MRAM arrangement can only be read from very slowly overall.

In order to avoid this disadvantage of the slow - and ultimately also unreliable on account of the parasitic

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currents - read-out of the MRAM arrangement of Fig. 8, an MRAM outlined in Fig. 9 has already been proposed, in which each individual memory cell comprises an MTJ layer sequence 4 and a selection transistor 5. A memory cell, surrounded by a broken line 6, is written to by sending corresponding currents through the word line WL2 and the bit line BL2. As a result, the MTJ layer sequence 4 of this memory cell is programmed correspondingly. For the read-out, select lines SL11 and SL13 are driven in such a way that the selection transistors 5 connected thereto are all turned off. By contrast, a voltage which is applied to a select line SL12 is such that the selection transistors 5 connected to said line turn on. A read signal is then applied to a select line SL22 of the select lines SL21 to SL23. Said read signal flows via the MTJ layer sequence of the memory cell surrounded by the broken line 6, since only the selection transistor of this memory cell is in the on state, while all the other selection transistors of the remaining memory cells are turned off. A signal indicating the state of the MTJ layer sequence 4, that is to say an information content "0" or "1", can thus be obtained at the output of the select line SL22.

Parasitic effects of adjacent memory cells can practically be precluded with the MRAM arrangement of Fig. 9. Consequently, the time for a read access is very short. What is disadvantageous about the MRAM of Fig. 9, however, is that the advantage of a high-density configuration is lost, since it is only possible to achieve an effective cell area of 8 F^2.

In order to resolve the above conflict between area requirement ("F^2") on the one hand, and fast read access without parasitic effects, on the other hand, thought has already been given, in the case of completely different memory arrangements, namely DRAM arrangements (DRAM = dynamic RAM),

to using so-called "shared contacts", in which one contact of a selection transistor is used by a plurality of memory cells, preferably by two memory cells, and area ("F^2") is thus saved. However, this solution cannot be employed for MRAMs, and so the above problem area has also not been solved hitherto.

Consequently, it is an object of the present invention to provide an MRAM arrangement which allows a rapid read access with a minimal area requirement.

In the case of an MRAM arrangement of the type mentioned in the introduction, this object is achieved according to the invention by virtue of the fact that in the memory cells an MTJ layer sequence and the drain-source path of a selection transistor in each case lie parallel to one another, so that the second select lines are formed by the source-drain paths of the selection transistors lying in series with one another.

Thus, in the case of the MRAM arrangement according to the invention, the selection transistors and the MTJ layer sequences of the individual memory cells lie parallel to one another. These memory cells or "basic elements" are then joined together to form chains, chains that run parallel to one another forming a memory matrix. The selection of a chain in such a memory matrix can be effected by a separate selection transistor. In other words, each individual chain is assigned a separate selection transistor at one end of the chain.

The MRAM arrangement according to the invention is written to in a customary manner by applying a corresponding signal in each case to the desired word and bit lines. During read-out, firstly a chain of the memory matrix is defined by means of the separate selection transistors. All the transistors of

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this chain are then activated apart from the transistor of the memory cell whose cell content is to be read. The transistor of the memory cell to be read thus remains turned off. If a current is then sent through the chain of this transistor to be read, the current flows solely through the MTJ layer sequence of the memory cell to be read and through all the selection transistors of the remaining memory cells of the chain. The cell content of the memory cell to be read can thus be determined.

The MRAM arrangement according to the invention is distinguished by a low area requirement: in the chain, given corresponding configuration, a memory cell comprising an MTJ layer sequence and a selection transistor lying parallel thereto has an effective cell area of 4 F^2. The separate selection transistor of a chain must be counted with this, which in turn requires an area of 4 F^2. For a chain having N memory cells, this results in an effective cell area for each memory cell of 4 F^2 (N + 1)/N.

It should be noted that in the case of N = 1, that is to say a chain comprising just one memory cell, an effective cell area of 8 F^2 is present, which corresponds exactly to the previously known solution comprising a series circuit of a selection transistor with an MTJ layer sequence. This means that the invention can be used particularly advantageously when, in an MRAM arrangement, the condition N > 1 is present, which applies, of course, to all the memory cells arranged in memory matrices.

The present invention, in a completely novel manner, departs from the previously customary principle of a series circuit comprising an MTJ layer arrangement and a selection transistor and proposes a novel concept in which the MTJ layer sequence

and the selection transistor in each memory cell lie parallel
to one another and are joined together to form chains.

The invention is explained in more detail below with reference
to the drawings, in which:

Fig. 1   shows a schematic circuit diagram of a chain of an
MRAM arrangement according to the present invention,

Fig. 2   shows a memory matrix of an MRAM arrangement according
to the present invention,

Fig. 3   shows a section of an exemplary embodiment of the MRAM
arrangement according to the invention,

Fig. 4   shows a plan view of the MRAM arrangement of the
exemplary embodiment of Fig. 3,

Fig. 5   shows an MTJ layer sequence in perspective,

Fig. 6   shows an illustration for elucidating the memory state
in an MTJ layer sequence in accordance with Fig. 5,

Fig. 7   shows an illustration of an MTJ layer sequence with a
word line and a bit line,

Fig. 8   shows a memory matrix with MTJ layer sequences in
accordance with figs. 5 to 7, and

Fig. 9   shows a memory matrix of a conventional MRAM
arrangement.

Figs. 5 to 9 have already been explained in the introduction.

In the figures, the same reference symbols are used in each case for mutually corresponding structural parts.

Fig. 1 shows a chain of an MRAM arrangement according to an exemplary embodiment of the present invention with selection transistors 5 and MTJ layer sequences 4 which lie parallel to one another in each case. In other words, lying above the drain-source paths of the selection transistors 5 is in each case an MTJ layer sequence 4, which, for their part, are connected in series with one another in the chain, as also holds true for the drain-source paths of the selection transistors 5.

Fig. 2 shows an exemplary embodiment of the MRAM arrangement according to the invention. Here a plurality of the chains shown in Fig. 1 with MTJ layer sequences 4 and selection transistors 5 lie parallel to one another, a separate selection transistor 7 also additionally being connected to each chain. Fig. 2 also additionally shows first select lines SL1 and row select lines RSL, which are in each case formed by the separate selection transistors 7 and the drain-source paths of the selection transistors 5.

If a specific memory cell, for example a memory cell Z2 of the chain shown in Fig. 1, is to be read from, then firstly the separate selection transistor 7 of said chain is turned on, while all the remaining separate selection transistors of the memory matrix remain turned off or nonconducting. The selection transistor 5 of the memory cell Z2 is then turned off in this chain by the application of a corresponding signal to the select line SL1 assigned to the memory cell Z2, while all the remaining selection transistors 5 of the chain are changed over to the on state. A current path I1, as is indicated schematically in Fig. 1 by a solid line with an

arrow, is thus present in the chain. This means that the resistance state of the MTJ layer sequence of the memory cell Z2 can readily be read out.

The process of reading into the MRAM arrangement shown in figs. 1 and 2 is effected in a customary manner. In other words, the MTJ layer sequences 4 in each case lie between bit lines BL and word lines WL, as is illustrated in a concrete exemplary embodiment in figs. 2 and 3, of which Fig. 3 illustrates a sectional illustration and Fig. 4 illustrates a plan view. The legend shown beside these figures applies to both figures in this case.

As can be seen from both Fig. 3 and 4, the MTJ layer sequences 4 lie between word lines WL and bit lines BL crossing the latter perpendicularly. By sending corresponding currents through the word lines WL and bit lines BL, MTJ layer sequences 4 located at the crossover points of such word lines and bit lines can be programmed as has been explained above.

The read-out is effected in the manner described above with reference to figs. 1 and 2: the separate selection transistor 7 of the chain with the memory cell to be read from is turned on, while all the other separate selection transistors 7 remain turned off. The selection transistor 5 of the memory cell to be read from in this chain is then turned off or made nonconducting by corresponding driving of the select line SL1, while all the remaining selection transistors of this chain are changed over to the on state by corresponding driving of their gates via the select lines SL1. In the memory cell with the turned-off transistor, that is to say in the memory cell to be read from, the read current then flows via the row select line RSL, that is to say via the drain-source paths of the selection transistors of the nonselected memory cells of

the chain and via the MTJ layer sequence 4 of the selected
memory cell with the turned-off selection transistor 5. In
this way, the cell content of the selected memory cell can be
read out rapidly and without parasitic currents.

Figs. 3 and 4 also illustrate the minimum feature sizes F of
the individual memory cells with 2 F in each case.

The invention thus enables a simply constructed MRAM
arrangement which departs completely from the previous concept
of a series circuit of selection transistor and memory cell
and instead provides a parallel circuit of selection
transistor and MTJ layer sequence. This different construction
makes it possible to ensure a high packing density, so that
the above-specified object of the invention is achieved in an
outstanding manner.

As can be seen from Fig. 3, in the MRAM arrangement according
to the invention, the bit lines BL run above the selection
transistors 5 and specifically above the gate electrodes
thereof at a distance therefrom.

Patent claims

1.   An MRAM arrangement comprising a multiplicity of memory cells (Z2) which are arranged in a memory matrix and each of which comprises at least one MTJ layer sequence (4) and a selection transistor (5), of which the MTJ layer sequences (4) are in each case located between word lines (WL) and bit lines (BL), which run at a distance from one another, the selection transistors (5) are connected to select lines (SL1) at their gates for reading from the memory cells and the MTJ layer sequences (4) are connected to second select lines (RSL), characterized
in that in the memory cells (Z2) an MTJ layer sequence (4) and the drain-source path of a selection transistor (5) in each case lie parallel to one another, so that the second select lines (RSL) are formed by the source-drain paths of the selection transistors (5) lying in series with one another.

2.   The MRAM arrangement as claimed in claim 1, characterized
in that the second select lines (RSL) of a chain of memory cells in the memory matrix lie in series with separate selection transistors (7).

3.   The MRAM arrangement as claimed in claim 1 or 2, characterized
in that the selection transistors (5) are connected to the first select lines (SL1) at their gates.

4.   The MRAM arrangement as claimed in one of claims 1 to 3, characterized

in that the minimum dimension of a memory cell is given by 4 F^2 where F denotes the minimum feature size of the technology used.

5.   The MRAM arrangement as claimed in one of claims 1 to 4, characterized
in that the first select lines (SL1) are routed above the gates of the selection transistors (5).

6.   The MRAM arrangement as claimed in claim 4 or 5, characterized
in that the first select lines (SL1) and the bit lines run parallel to one another.